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Abstract

Floorplanning is an important physical design step for hierarchical, building-block design methodology. When the circuit size get increases the complexity of the circuit also increases. To deal with the increasing design complexity the intellectual property (IP) modules are mostly used in floorplanning. This paper presents a Hybrid particle swarm optimization algorithm for floorplanning optimization. Here B*tree is used at the initial stage in order to avoid overlapping of modules and later, PSO algorithm along with the concept of crossover and mutation from Genetic algorithm is used to get optimal placement solution. The main objective of floorplanning is to minimize the chip area and interconnection wire length. The Experimental

results on Microelectronic Center of North Carolina (MCNC) benchmark circuits shows that our algorithm performs better convergence than the other methods.

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Index Terms

Computer Science

Intregarted Circuit

Keywords

Hybrid Particle Swarm Optimization (hpso) Genetic Algorithm (ga) Crossover
Mutation

Microelectronic Center Of North Carolina (mcnc)

Very Large Scale Integrated Circuits(vlsi)