{tag} {/tag}
International Journal of Computer Applications

Volume 40 - Number 4

Year of Publication: 2012

Authors:
Masoud Shiroie

Karim Mohammadi

10.5120/5029-7177
{bibtex}pxc3877177.bib{/bibtex}

Abstract

Remarkable advantages of asynchronous circuits in comparison with their synchronous counterparts results in vast effort in designing such circuits. This paper proposes optimized asynchronous circuit design approach by exploiting potent evolutionary circuit design method. The evolutionary algorithm applies fast and accurate hazard detection technique as a fitness function. Outcomes of proposed method in designing fundamental mode asynchronous circuit in comparison with previous methodologies reveal its notable advantages like, multi level circuit design with lower number of gates which results in lower area, lower power consumption and lower cost. Experimental result demonstrate that the proposed method reduces number of gates about 16.81%.

References

- Hauck, S. “Asynchronous design methodology: an overview”, In Proceeding of the IEEE, Vol. 83, No. 1, pp. 69-93,
- J. Sparso, S. Furber “Principles of asynchronous circuits design – a system perspective”, Springer Publisher, 2001.

- P. A. Beerel and T. Meng, “Automatic gate-level synthesis of speed independent circuits”, IEEE International Conference on Computer-Aided Design, pp. 581-586, Nov. 1992.
- E. Brunvand, R. F. Sproull, “Translating concurrent programs into delay-insensitive circuits,” IEEE International Conference on Computer-Aided Design, pp. 262-265, NOV. 1989.
- S. H. Unger, “Asynchronous sequential switching circuits”, New York Wiley-Interscience, 1969.
- J. Frackowiak, “Methoden der analyse und synthese von hasardarmen schaltnetzen mit minimalen kosten I,” Elektronische Informationsverarbeirung und Kyberneitik, vol. 10, no. 213, pp. 149-187, 1974.
- D. S. Kung, “Hazard-non-increasing gate-level optimization algorithms,” IEEE International Conference on Computer-Aided Design, pp. 631-634, 1992.
- S. M. Nowick, D. L. Dill “Exact two-level minimization of hazard-free logic with multiple-input changes”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no. 8, August 1995.
- L. Lavagno, K. Keutzer, and A. Sangiovanni-Vincentelli, “Algorithms for synthesis of hazard-free asynchronous circuits,” In ACM/IEEE Design Automation Conference, pp. 302-308, 1991.
- M. Theobald, S. M. Nowick, T. Wu, ”Espresso–hf: a heuristic hazard–free minimizer for two–level logic”, pp. 71–76, 1996.
- J. Rutten, M. Berkelaar, “Efficient exact and heuristic minimization of hazard-free logic,” In Proceeding of International Conference of Computer Design (ICCD), pp. 152–159, 1998.
- B. Lin, S. Devadas, “Synthesis of hazard-free multi-level logic under multiple-input changes from binary decision diagrams,” In proceeding of International Conf of Computer-Aided Design (ICCAD), pp. 542–549,1994.
- F. Shi, “Removing hazards in multi-level logic optimization for generalized fundamental-mode asynchronous circuits”, IEEE International Conference on Computer Design, pp.640-645, 2008.
- E. C. Tan, M. H. Ho, “Matrix method to detect logic hazards in combinational circuits with EX-OR gates”, Journal of Universal Computer Science, vol. 5, no. 11 , pp. 765-776, 1999.
- I. Beister, “A unified aproach to combinational hazards”, IEEE Transaction on Computers, pp. 566-575, June 1974.
- Jens Sparsø, ” Asynchronous circuit design”, Technical University of Denmark, 2006.
- J.A. Brzozowski, Z. Esik, Y. Iland ,“Algebras for hazard detection”, 31st IEEE International Symposium on Multiple-Valued Logic, pp.3-12, 2001
- M.K. Michael, S. Tragoudas, “Generation of hazard identification functions”, Fourth International Symposium on Quality Electronic Design, pp. 419- 424, 24-26 March 2003.
- I. Kajitani, T. Hoshino, M. Iwata, Higuchi, T. Higuchi, “Variable length chromosome GA for evolvable hardware”, IEEE International Conference on Evolutionary Computation, pp. 443-447, 1996.
- E. Stomeo, T. Kalganova, C. Lambert, “Generalized Disjunction Decomposition for Evolvable Hardware,” IEEE Transactions on Systems, Man, and Cybernetics, Part B: Cybernetics, vol.36, no.5, pp.1024-1043, 2006.
- T. Higuchi, M. Murakawa, M. Iwata, I. Kajitani, Weixin Liu, M. Salami, “Evolvable hardware at function level”, IEEE International Conference on Evolutionary Computation, pp.

187-192, 1997.

- J. Lee, J. Sitte, “A gate-level model for morphogenetic evolvable hardware,” IEEE International Conference on Field-Programmable Technology, pp. 113-119, 2004.
- J. Lee and J. Sitte, “Gate-level Morphogenetic Evolvable Hardware for Scalability and Adaptation on FPGAs,” First NASA/ESA Conference on Adaptive Hardware and Systems, pp. 145-152, 2006.
- J. A. Walker, J. F. Miller, “The automatic acquisition, evolution and reuse of modules in Cartesian genetic programming “, IEEE Transactions on Evolutionary Computation, vol. 12, pp. 397-417, 2008.
- R. M. Fuhrer, S. M. Nowick, M. Theobald, N. K. Jha, B. Lin, and L. Plana, “Minimalist: An environment for the synthesis, verificationand testability of burst-mode asynchronous machines,” Columbia University, NY, Tech. Rep. TR CUCS-020-99, July 1999.

Index Terms

Computer Science Integrated Circuits

Keywords

Hazard Evolutionary algorithm Burst mode machine Asynchronous Genetic programming