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Abstract

ALU is one of the most important components in a microprocessor that carries out the arithmetic and logical operations. This paper highlights the techniques in designing a low power ALU in nanometer CMOS. Different 10 transistor full adders are compared and chosen the Full adder with least power dissipation to obtain low power and area efficient ALU. The power is reduced by 78% when compared to the existing ALU which is designed using XOR based Full adder. The proposed design does not compromise with the performance as the full adder delay is less. The functionality of the design remains the same despite the temperature and voltage variations. The power dissipation for different temperatures ranging from -50 0C to +50 0C has been observed. The ultimate goal is to design an ALU with the least number of transistors thereby decreasing the area and power consumption in the overall circuit that takes shape at the end.

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Index Terms

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