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Abstract

This article is based on the application of heuristic algorithms to minimize the average power consumption in a VLSI circuit. The idea is to find the optimum layout and temperature for a 3 stage ring oscillator with minimal dynamic average power. The objective function is the same as average power (P_{avg}) of 3 stage ring oscillator with 6 CMOS inverters that depends on the temperature and the two different group of channel widths for NMOSs and PMOSs. ($W_1=W_3=W_5$ and $W_2=W_4=W_6$). These parameters make a three dimensional search space which is explored by search agents of algorithms. Motivated by the convergence of Modified Shuffled Frog Leaping Algorithm (MSFLA), Genetic Algorithm (GA) and the link of MATLAB with HSPICE Software the minimized average power of 3 stage ring oscillator is obtained. Based on MSFLA, Fuzzy-MSFLA, GA, and Fuzzy-GA algorithms the best resulting for P_{avg} in 0.18 μ m Technology and the supply voltage of 5v is 1.19 μ W based on Fuzzy-MSFLA.

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Index Terms

Computer Science

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3 stage CMOS ring oscillator minimal average power optimum layout and temperature
Fuzzy-MSFLA MSFLAF

GA

and Fuzzy-GA.