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Abstract

A Low Noise amplifier is one of the most commonly used components in analog and digital circuit designs. Low voltage and low power Low Noise amplifier design has become an increasingly interesting subject as many applications switch to portable battery powered operations. An electronic amplifier is an electronic device that increases the power of a signal. This design techniques is needed to allow amplifiers to maintain an acceptable level of performance when the supply voltages are decreased is immense for maintain low noise with high gain. The low-noise amplifier is a special type of electronic amplifier used to amplify very weak signals captured by an antenna. This paper presents a technique for substantially reducing the noise of a CMOS low noise amplifier implemented in the cascade inductive source degeneration topology. This 2. 4 GHz Two Stage CMOS 130nm RF Low Noise Amplifier is optimize for low noise at low current with very low power consumption. In this proposed design work the two stage cascade low noise amplifier is used to achieve noise 28 dB, input return loss of >10 and output return loss of > -10 at 1. 3 supply voltage.

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Index Terms

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Keywords

CMOS two stage cascode low noise amplifier noise gain and power.